Cisco- M-CMTS deep dive

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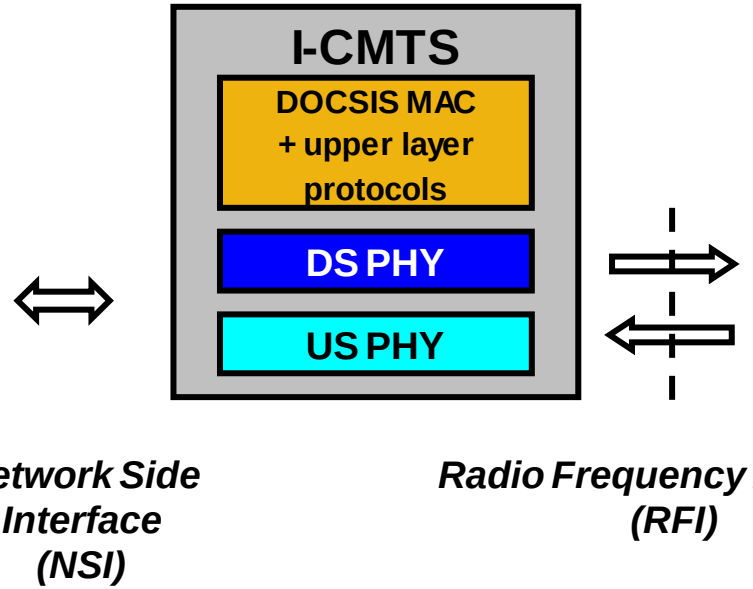
Agenda

- 1. M-CMTS introduction- Concepts and Architecture
- 2. DEPI - Downstream External Phy Interface
- 3. DEPI CP (Control Plane)
- 4. Timing (DOCSIS)
- 5. M-CMTS hardware components
  - MC3G60
  - RFGW-10
- 6. DEPI CP configuration steps
  - uBR10012
  - RFGW-10
- 7. DEPI HA
- 8.L2 CIN Interconnect

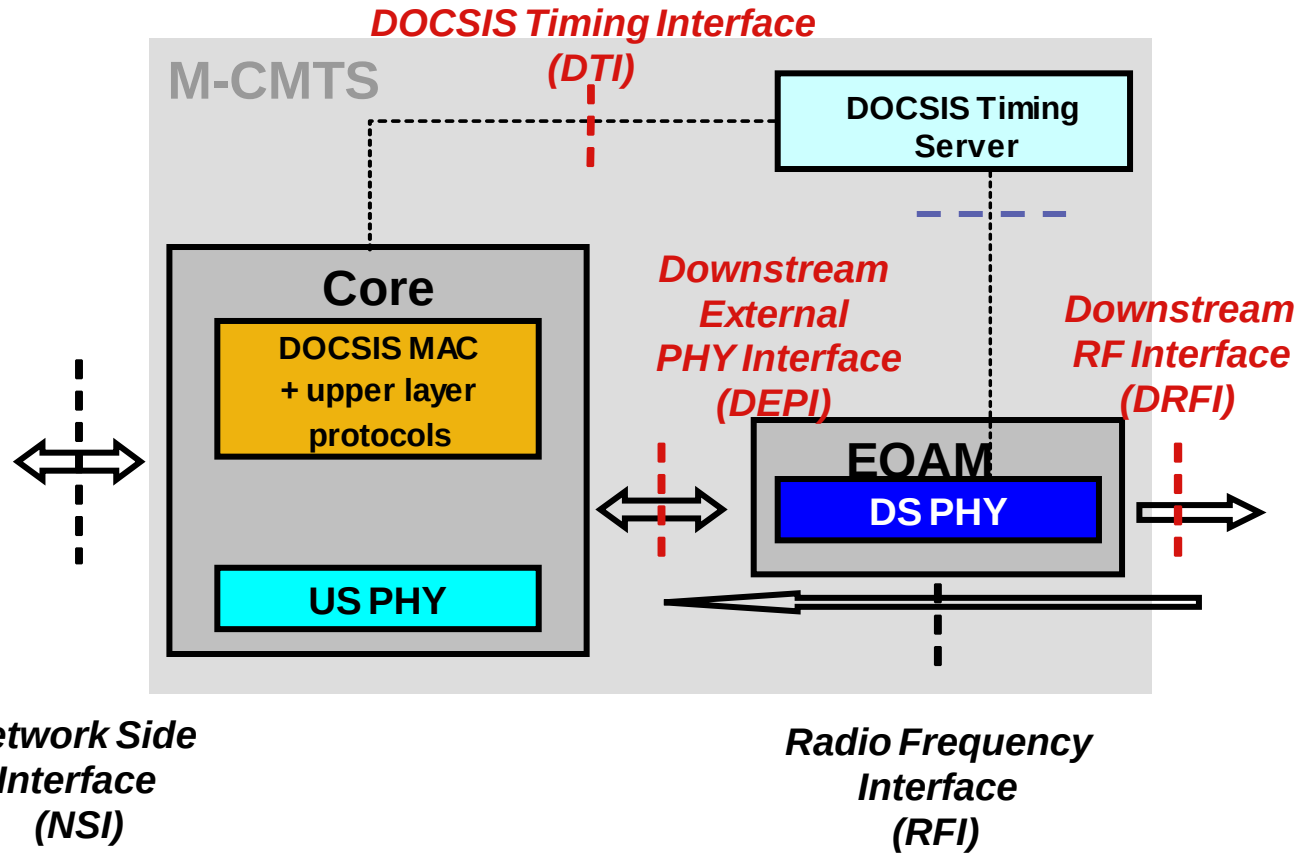
M-CMTS introduction- Concepts and Architecture

Differences from Integrated-CMTS (I-CMTS)

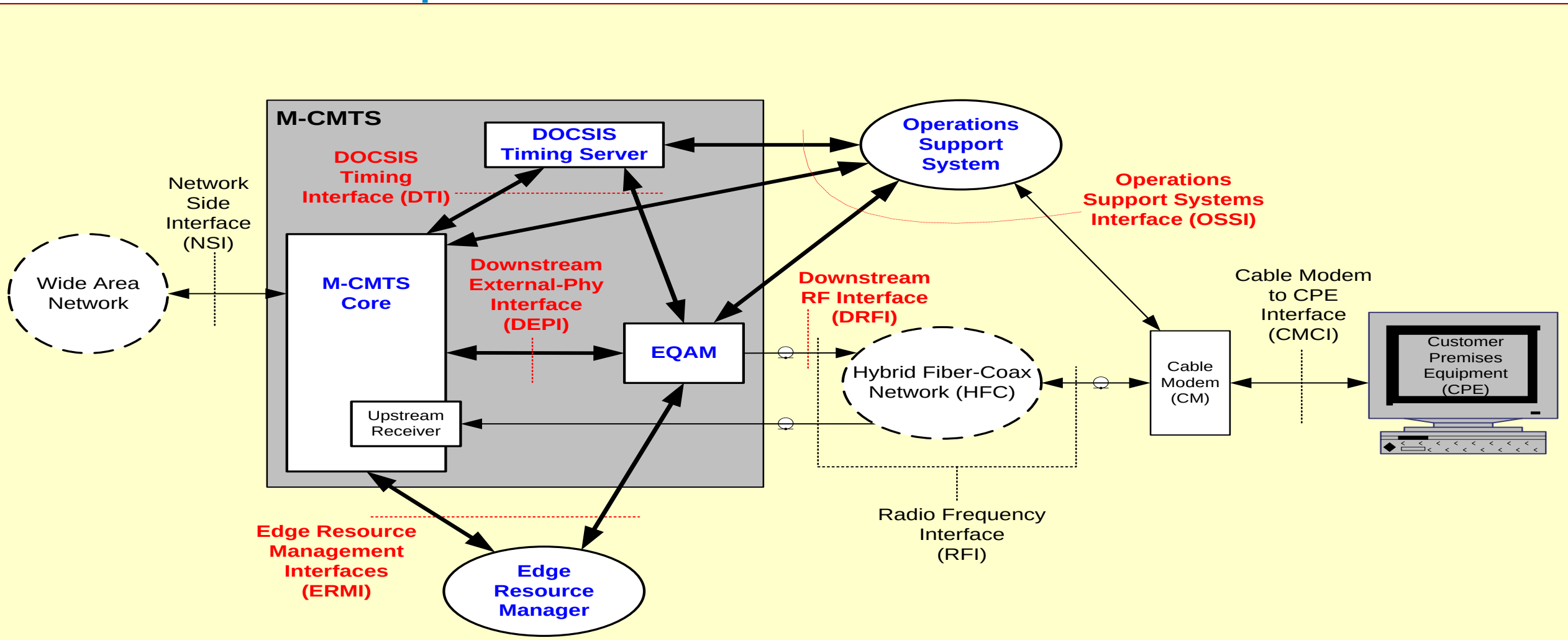
- MAC, DS PHY and US PHY Functions are Co-located on the Same Line Card
- Fixed Ratio between DS and US Ports



- **External DS PHY (Separate MAC and PHY)**
- **Flexible Ratio between DS and US Ports**
- **Timing Server to Keep the Two Boxes in Synch**



M-CMTS Components and Interfaces

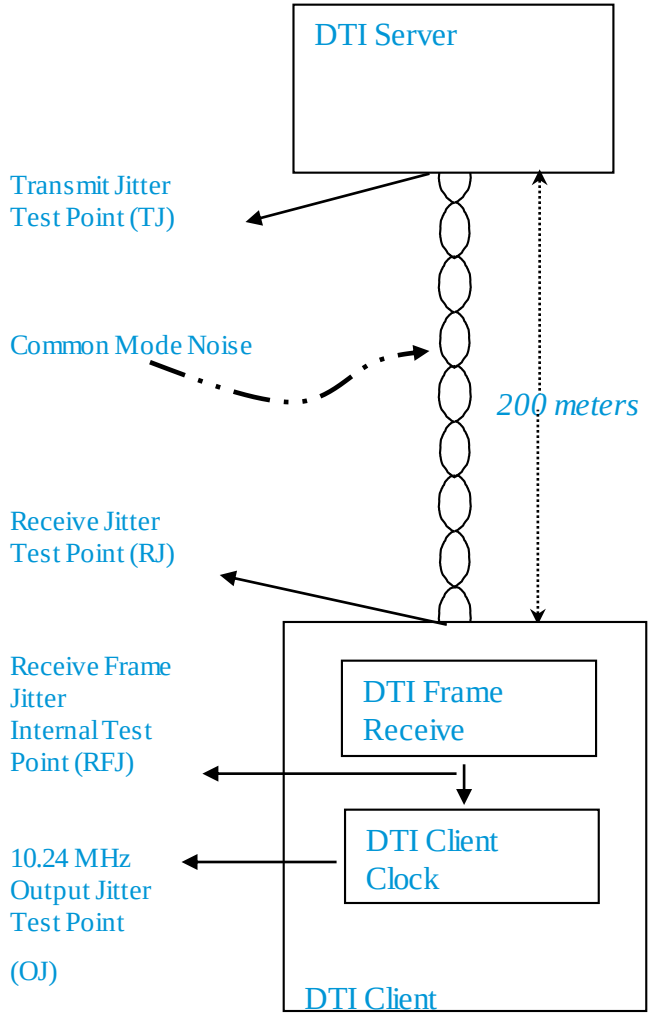


M-CMTS Components

- Edge Resource Management Interface (ERMI)
  - Not used in current M-CMTS implementations (CCAP)
  - Will be used for allocating QAM channels between DOCSIS and VOD.
- DOCSIS RF Interface (DRFI)
  - RF specification for a multi-channel downstream that is shared between M-CMTS and DOCSIS 3.0
- Operations Support Systems Interface (OSSI)
  - SNMP MIBs for managing M-CMTS

DOCSIS Timing Interface (DTI)

- DTI provides:
  - 32 bit timestamp at each device time aligned to 5 ns (same site).
  - 10.24 MHz clock.
- DTI Server with GPS provides:
  - Clock traceable to Stratum 1
  - TOD (Time of Day) & GPS co-ordinates available.
- A DTI Server connects point to point with a DTI Client.
  - 5Mbps rate. 200 meters. CAT5.
  - 10 kHz frame rate. Full Duplex.



End-to-End Cisco DOCSIS 3.0 Solution

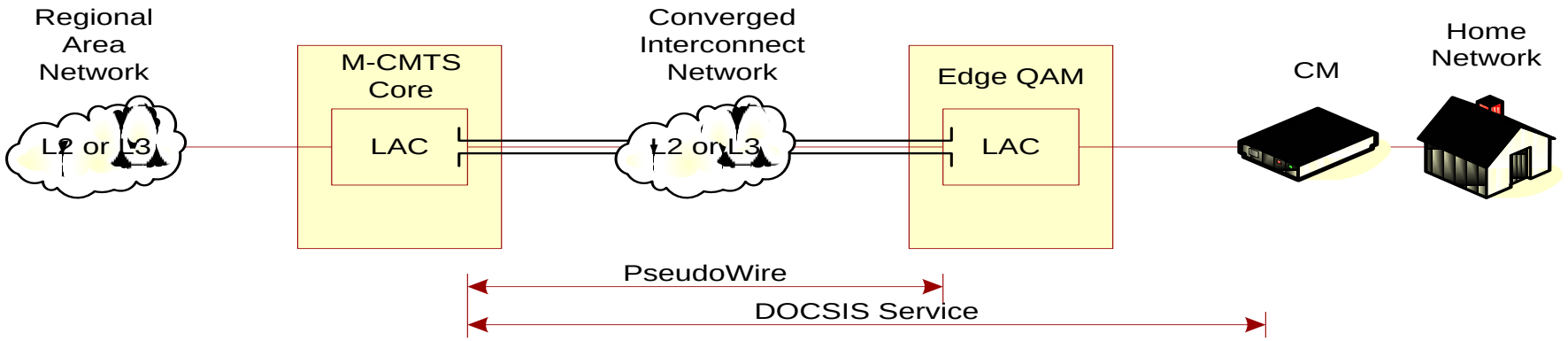
- M-CMTS architecture allows use of Universal Edge QAM supporting both DOCSIS and Video services to maximize QAM channels per port
  - Lowers cost per QAM and reduces space and power for all services
- uBRMC3GX60V can co-exist with MC5X20H and MC20X20V Line Cards in uBR10012
  - Eases migration to full-scale DOCSIS 3.0
- uBR10012 with MC3GX60V and RFGW-10 will meet many of the key requirements of the emerging CCAP specifications

DEPI - Downstream External Phy Interface

What is DEPI?

- DEPI (Downstream External PHY Interface)
  - IP Tunnel between M-CMTS MAC and EQAM PHY
  - Data path for DOCSIS frames
  - Control path for session setup/maintenance/tear down
  - Base protocol L2TPv3 [RFC 3931]
    - Generic protocol for creating a pseudowire

Downstream External PHY I/F (DEPI)



- DEPI is based upon a L2TPv3 (RFC 3931) pseudowire that exists in the downstream direction between a DOCSIS MAC in a M-CMTS Core and a DOCSIS PHY in an EQAM.
  - The CIN (Converged Interconnect Network) may be a L2 or L3 network.
- DEPI uses two new pseudowire types:
  - D-MPT (DOCSIS MPEG Transport) for MPEG frames.
  - PSP (Packet Streaming Protocol) for packets.
  - M-CMTS Core/EQAM must support MPT or PSP.

DEPI Modes

- Two basic tunneling techniques
- D-MPT
  - Transports 188-byte MPEG-TS packets in the L2TPv3 payload
    - Sub-header for sequence number
  - Encapsulation of DOCSIS frames into MPEG-TS done at M-CMTS
- PSP
  - Transports DOCSIS frames in the L2TPv3 payload
  - Encapsulation into MPEG-TS done at EQAM

DEPI D-MPT (EQAM Data Path)

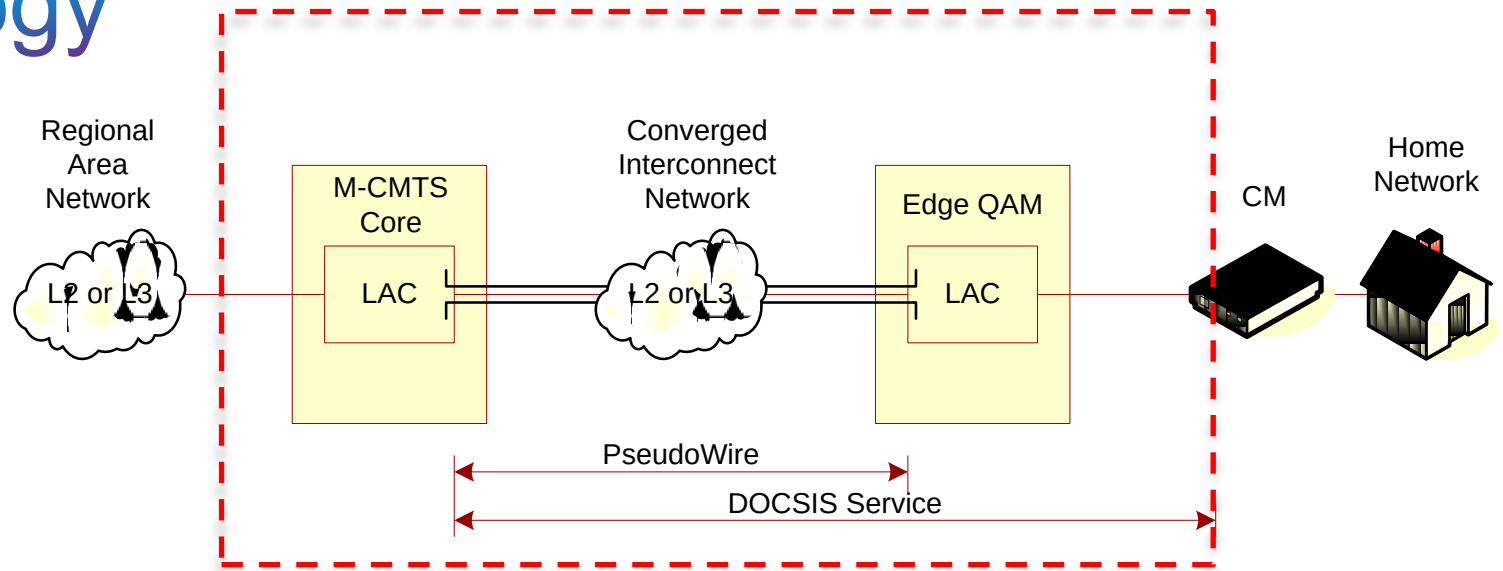
- EQAM searches incoming D-MPT frames for DOCSIS SYNC messages
- Corrects the timestamp value in messages based upon the EQAM's internal DOCSIS timestamp, which has been derived from DTI
- D-MPT frames copied to QAM channel without further interpretation or modification
- For DOCSIS frames where the MAP is embedded into the stream
- Network latency or jitter is not a concern
- Does not allow for QoS differentiation among various types of traffic
- Certain network conditions/architectures may reduce network delay/jitter [CIN]
- MUST support PSP mode, D-MPT mode or both
- One priority level for D-MPT per session

DEPI D-MPT (M-CMTS Data Path)

- D-MPT mode encapsulates all DOCSIS traffic into a single DEPI flow
- (EQ)MUST support PSP mode, D-MPT mode or both
- Only one priority level for D-MPT per session
- M-CMTS generates SYNC messages
  - Included in D-MPT payload (Starts at 6th byte of MPEG-TS frame)
- SYNC need not reflect current timestamp (Can be zero)

DEPI Control Plane

Topology



- M-CMTS & EQAM known as LAC (L2TP Access Concentrator)
- Considered peers
- L2TP nodes, or L2TP Control Connection Endpoints (LCCE)
- Supports both data and control path
- Control Connection established first
- Multiple sessions may be bound to single control connection

Addressing

- M-CMTS should use EQAM IP and TSID of QAM channel
- M-CMTS MUST establish only one active control connection for each LCCE pair
- M-CMTS/EQAM MUST support single session per QAM
- Uses only one pseudowire type
- Unique L2TPv3 session ID per session
- Only one session per QAM (M-CMTS)
- L2TPv3 allows optional use of UDP ports (Not supported)

Control Message Format

- Based on RFC 3931 with extensions for DOCSIS
- Specific QAM AVPs added for DOCSIS

Signaling

Supported L2TPv3 messages for DEPI CP

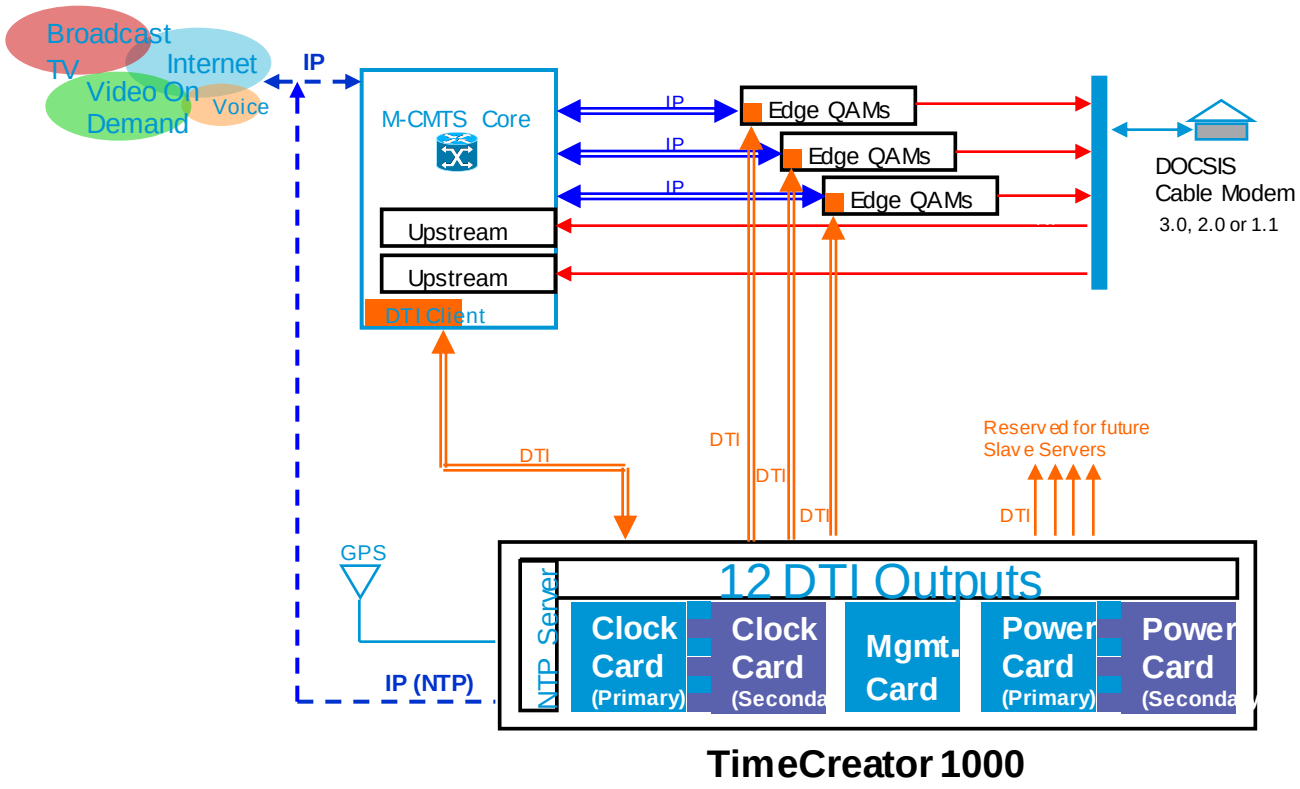
#	Mnemonic	
Control Connection Management		
1	SCCRQ	Start-Control-Connection-Request
2	SCCRP	Start-Control-Connection-Reply
3	SCCCN	Start-Control-Connection-Connected
4	StopCCN	Stop-Control-Connection-Notification
5	HELLO	Hello
20	ACK	Explicit Acknowledgement
Session Management		
10	ICRQ	Incoming-Call-Request
11	ICRP	Incoming-Call-Reply
12	ICCN	Incoming-Call-Connected
14	CDN	Call-Disconnect-Notify
16	SLI	Set Link Info

Required and Optional AVPs

DEPI Control Message	DEPI Mandatory AVPs	DEPI Optional AVPs
ICRQ	DEPI Resource Allocation Request DEPI Local MTU DS QAM Channel DOCSIS SYNC Control	Local UDP Port DPR Session Type
ICRP	DEPI Resource Allocation Reply DEPI Remote MTU EQAM Capabilities DS QAM Channel Frequency DS QAM Channel Power DS QAM Channel Modulation DS QAM Channel J.83 Annex DS QAM Channel Symbol Rate DS QAM Channel Interleaver Depth DS QAM Channel RF Mute	
ICCN		DS QAM Channel Frequency DS QAM Channel Power DS QAM Channel Modulation DS QAM Channel J.83 Annex DS QAM Channel Symbol Rate DS QAM Channel Interleaver Depth DS QAM Channel RF Mute
SCCRQ		DEPI Redundancy Capabilities
SCCRP		DEPI Redundancy Capabilities
CDN		DEPI Result Code
StopCCN		DEPI Result Code
SLI		DS QAM Channel DOCSIS SYNC Control DS QAM Channel Frequency DS QAM Channel Power DS QAM Channel Modulation DS QAM Channel J.83 Annex DS QAM Channel Symbol Rate DS QAM Channel Interleaver Depth DS QAM Channel RF Mute DEPI Result Code DPR Session Status

DOCSIS -Timing

Deployment Scenario
Initial Deployment (Small Site)



TimeCreator 1000

DEPI Hardware Components – MC 3G60

MC3G60 Overview

- An M-CMTS LC that plugs into an RF slot of UBR10012
- 72 DS channels and 60 US channels
  - 20 US connectors – physical connectivity identical to 520/2020
  - Six GE ports for M-CMTS output: organized in three 1+1 pairs
- 3X US density and 14X DS density when compared to 520 LCs
- Increased configuration flexibility
  - Up to 15 MAC Domains
  - 1-24 DS channel BG sizes
- Line rate performance
- Full DOCSIS 3.0 and M-CMTS Compliance

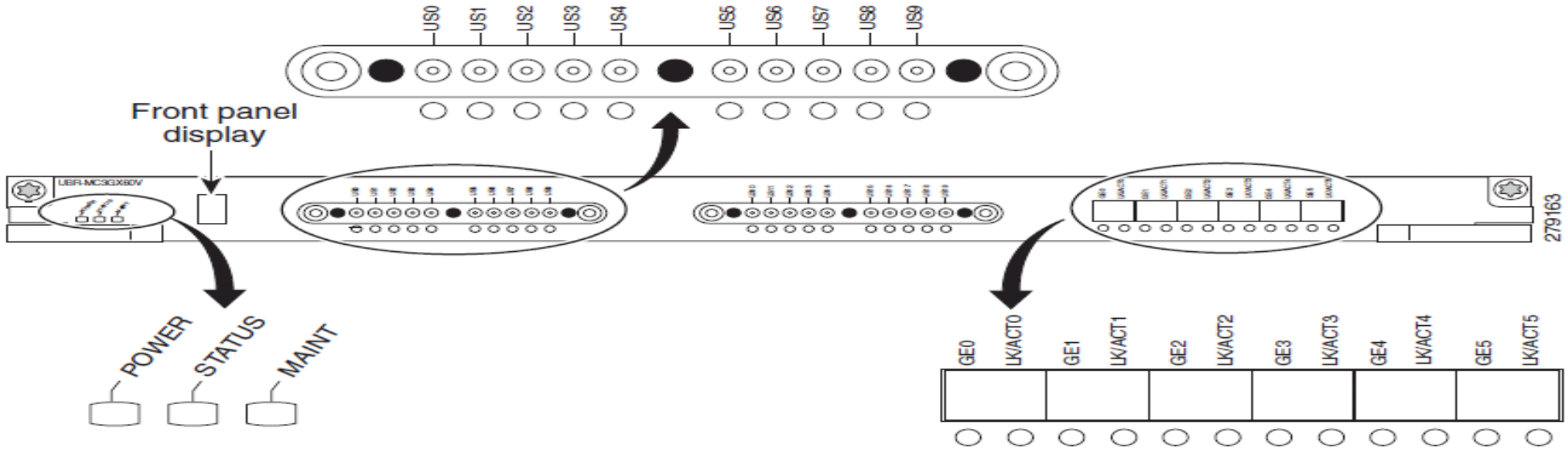
MC3G60 in UBR10012 Chassis

- UBR10012 chassis can include
  - Up to 8 MC3G60 LCs
  - A mix of older LCs and/or up to six Modena SPAs
- UBR10012 chassis with MC3G60 must include
  - PRE4 with SIP-600 (Spumoni)
  - Up to 2 10GE SPAs for backhaul connectivity
    - Other backhaul SPAs are supported but not practical given LC's density
  - DTCC
    - Dual DTCCs are recommended, even when connected to a single DTI server
- Power Supplies
  - MC3G60 total power consumption exceeds 520 LC but smaller then MC2020

uBR-MC3GX60V Broadband Processing Engine

MC3GX60V

- An M-CMTS LC that plugs into an RF slot of UBR10012
- DS ports are Six Gigabit Ethernet (GigE) Small form-factor pluggable (SFP) ports, organized in three pairs for 1+1 network connectivity redundancy
- Front panel display is 4 character LCD displaying license installed on card
- US ports are layed out exactly the same as the MC5x20H & MC20x20V
  - Uses UCH2 holders in 2 blocks of 10 upstreams



MC3GX60V License Front Panel Display

- Front panel display has 4 characters to display license installed on the MC3GX60V
- MC3GX60V comes with a HW base and a min 16x16 license
- Can purchase US and DS licenses separately to meet your network needs
- Examples are shown in the table below

Front Panel Display	Downstream	Upstream
3G60	72	60
2G40	48	40
1G20	24	20
3314	33	14
2010	20	10

MAC Domain Structure in MC3GX60V

- MC3GX60V has 15 MAC domains
- Any DS from any of the controllers can be added to a MAC domain
  - Each DS can only be associated with one MAC domain for primary services
- Can only associate DS from the SAME Linecard to a MAC domain
- MAC domain can have 1 US to 8US
- Each MAC domain has by default 4 US associated
- US channels stacked on 1 physical connector can be shared across MAC domains
  - Each US channel though can only be associated to 1 MAC domain
- Each US within a MAC domain can be associated to any of the US physical connectors

MC3G60 in UBR10012 Chassis Rules

- The MAC Domains defined on MC3GX60V LCs cannot include DS channels from Modena SPAs
- DS can only be bonded within Linecard
- DS can only be bonded within controller- *Future release to support this feature*
- Licensed DS ports can be on any of the controllers up to the License limit
- Licensed US ports can be on any connector / MAC domain up to license limit
- In EuroDOCSIS mode, it is possible to oversubscribe the DS (get a warning to tell you of this)

US Connectivity

- MC3G60 includes 5 Broadcom 3142 Phy Receiver ICs
  - Each 3142 IC supports 12 US channels physically attached to a set of 4 US connectors
  - Flexible mapping of 12 US channels to any of 4 connectors in the associated set
  - 0-12 US channels (frequencies) can be stacked on any connector
- 15 MDs defined in default configuration
  - Each MD with 4 US channels and one connector
  - Connectors 3,7,11,15,19 are unused
- 5 MHz-85 MHz US frequency range
- MC3G60 supports 2 logical channels per physical channel

Upstream Stacking

- The Cisco uBR-MC3GX60V cable line card upstreams are in connector blocks
  - 4 physical connector inputs will share 12 PHY receivers.
  - upstream channel-to- physical connector assignment is flexible enough to provide any combination of 1 to 12 channels per connector from the 4-connector bundle.
- This means four separate connectors could provide
  - 3 US stacked on all 4 connectors
  - 12 US stacked on 1 connector (other 3 in the block will not be used)
  - Any other combination across the 4 physical connectore as long as the total is a max of 12 channels.
- Default configuration is 4 US stacked on first 3 connectors in the block and last connector not used

Default Upstream Design

- To keep symmetry with all other Cisco LC, the default domain will have 4 US
- On MC3GX60V this will mean that we have 15 MAC domains with 4 US per domain = total of 60 US
- Each domain will be stacked on 1 physical port (4 US per port)
- Therefore only 15 US ports are used by default

  Due to the 12 US recievers per block(4US)

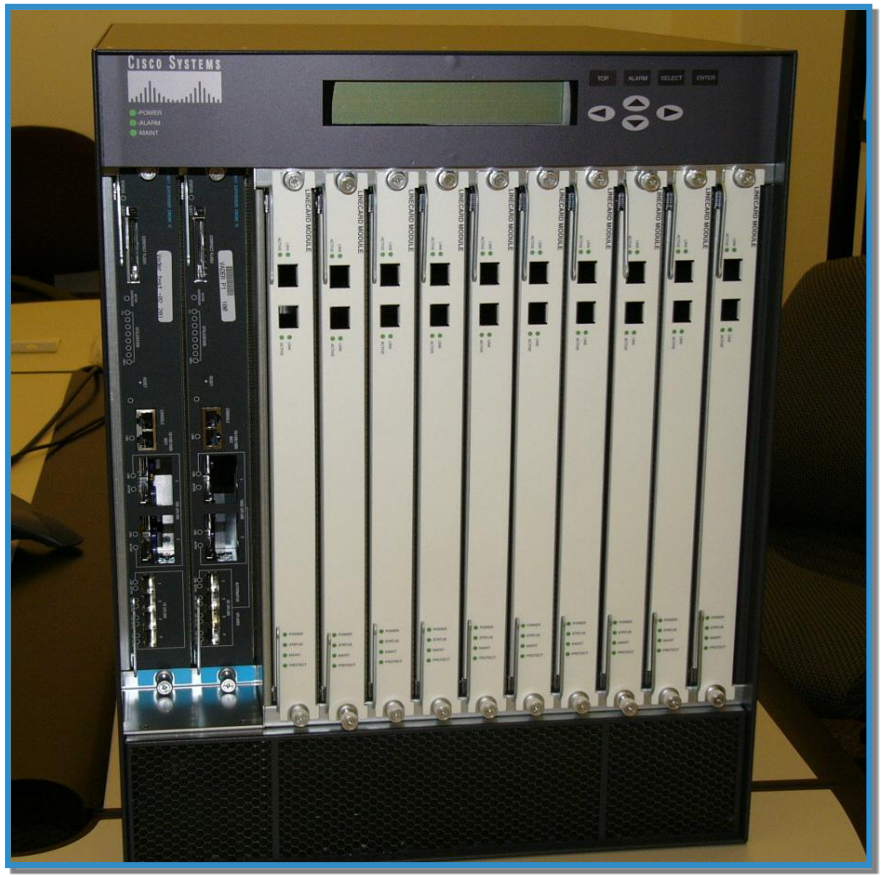
  => every 4th port not used
- Default US ports used

  0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18

  US3, US7, US11, US15, US19 not used

DEPI Hardware Components – RFGW-10

RF Gateway (RFGW-10)



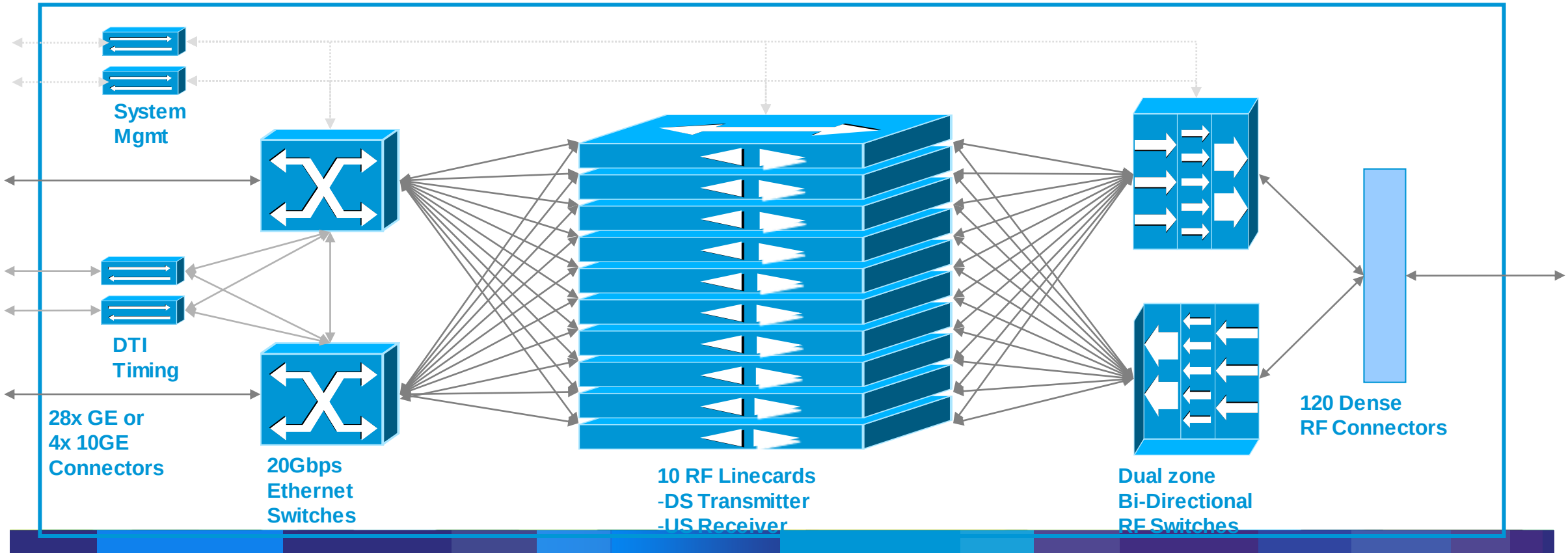
- Universal EQAM chassis
  - DOCSIS 3.0 & M-CMTS support
  - VOD and SDV support
- Capacity / Density
  - 480 QAM in current HW scaling to <3000 QAM in FY12
- Specifications
  - 12 slot chassis
  - 20Gbps+ backhauls (2*10GE or n*GE)
  - Front-to-back airflow
  - Dual-zone Integrated RF switch
  - Cable Once, Dense connectors
  - Linecard <500ms failover
- Extensive software and hardware HA
- Evolution path to multiple form factors

RFGW-10 Rear View

- 4 Fan, Dual Vane Fan Tray
  - Cooling for up to 4400 W
  - Hot Swappable
  - Temperature Sensing Variable Speed
- (12) RF Switch Cards
  - 120 Bi-Directional RF (Coax) ports – *5 to 1GHz*
  - Dense-style coaxial connectors (RU-1459)
  - Dual Zone RF Switch - *N+1 (DS), M+1 (US)*
  - Two slots in the chassis can be designated as protect slots, each with its own redundancy group.
- (2) Redundant DC Power Supplies
  - Load sharing
  - Fully Redundant
- (2) DTI / System Timing Card Slots
  - M-CMTS Redundant External DTI Interface
  - Provides internal system and DOCSIS clocking

RFGW-10 Functional Block Diagram

- **The RFGW-10 has a fully redundant architecture;**
  - **2x power supplies**
  - **2x 20Gbps Ethernet switches**
  - **2x synchronization cards**
  - **10x universal RF linecard slots**
  - **Dual-zone bi-directional RF switch.**



DEPI CP configuration steps

DEPI CP Configuration Steps (uBR10012)

DEPI Control Plane (DEPI Protocol Mode) NO HA

- Create L2TP Class
- Create DEPI class
- Create depi-tunnel
    1. L2TP class association
    2. DEPI class association
    3. Destination IP (IP of EQAM)
- Assign RF channel of Modular Controller to DEPI tunnel and EQAM TSID

Optional (But highly recommended)

- Create VRF for 3G60 and WB SPA GE
    - Prevent DEPI IP space from being advertised by routing protocols
- Configure DEPI Latency Measurement (DLM)
- Verification

DEPI CP Configuration Steps (RFGW-10)

DEPI Control Plane (DEPI Protocol Mode) NO HA

- Create L2TP Class
- Create DEPI class
- Create depi-tunnel
    1. L2TP class association
    2. DEPI class association
    3. Destination IP (IP of CMTS 3G60 / WB SPA)
- Configure RFGW-10 QAM interface(s) to DEPI “remote learn” mode
- Configure unique TSID for RFGW-10 QAM interface
- Configure DEPI tunnel for RFGW-10 QAM interface
- Verification

DEPI DLM (depi latency measurement)

DEPI Latency Measurement (DLM)

- Used to measure the delay introduced by the CIN
- The CIN Delay is used in the MAP advance calculation
- Two types of DLM packets, Ingress and Egress
- Ingress is mandatory, Egress is optional
- EQAM advertises what it supports during Data Session establishment
- RFGW-10 only support Ingress in the Blackstone (SQ3 in TME lab)release
- Supports 3G60 N+1 LCHA
- DLM responses are processed by the 3G60 CPU
  - This differs from the SPA, where responses are processed by the PRE CPU
- MAP advance CIN delay updated if DLM moving average differs by >/=75 usec

DLM Configuration

- Configurable on each Modular Primary channel

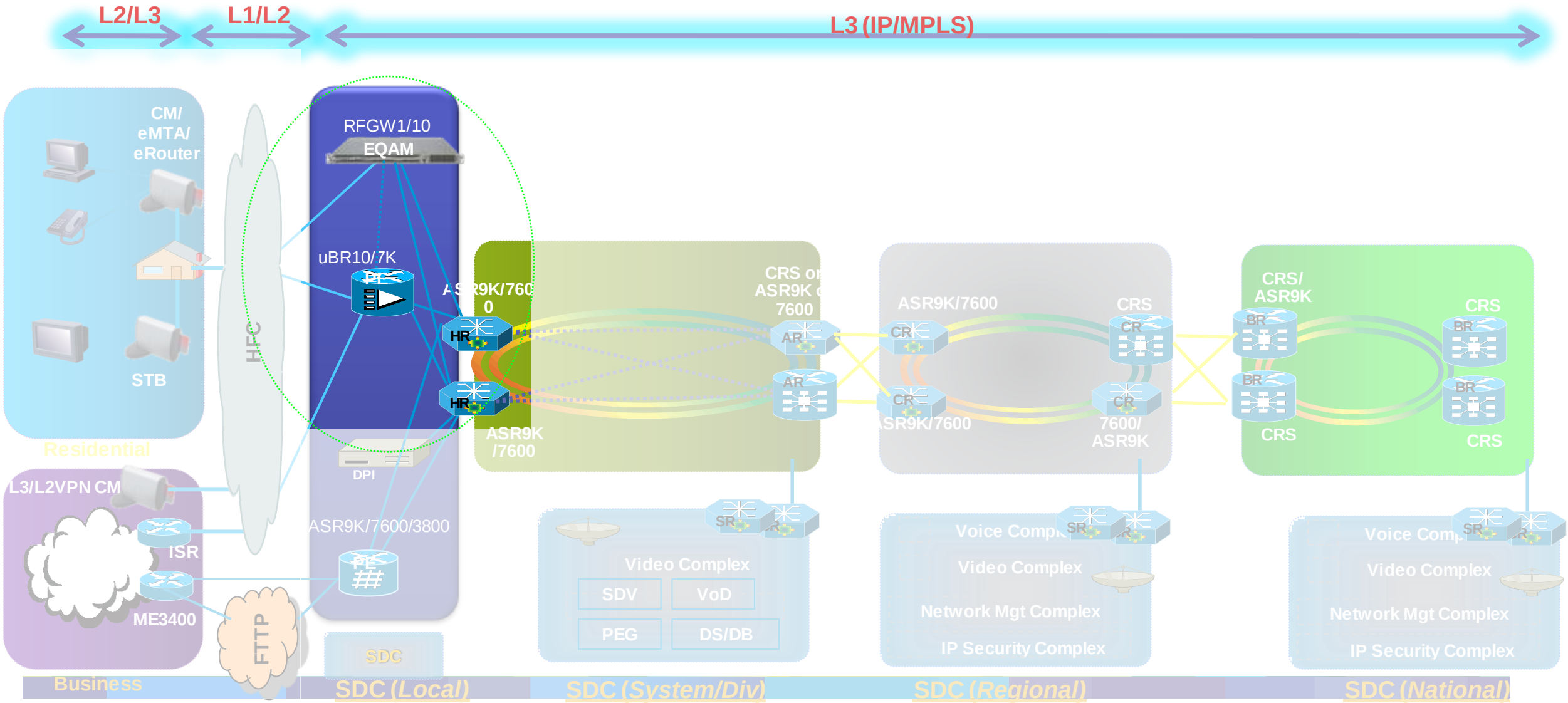
```
controller Modular-Cable 6/0/0
 rf-channel 0 cable downstream channel-id 1
 rf-channel 0 frequency 432000000 annex A modulation 256qam interleave 12
 rf-channel 0 network-delay auto sampling-rate 1
 rf-channel 0 depi-tunnel DEPI_600 tsid 15101
 rf-channel 0 rf-power 52.0
 no rf-channel 0 rf-shutdown
```

- Sampling-rate specifies how often a request is sent
- No configuration is necessary on the EQAM
- Measurement data can be viewed using show command

```
show interface Modular-Cable 6/0/0:0 dlm
```

DEPI HA-High Availability

CESNA IP/NGN DEPI Inclusion



CESNA & DEPI M-CMTS Connectivity Comparison

		Direct (Back2Back)	Indirect (IP Network)	Hybrid
1	EQAM Impact	Requires 2x1GE ports for 1G traffic (port wasted)	Requires 1x1GE ports for 1G traffic (no port wasted)	Requires 1x1GE ports for 1G traffic (no port wasted)
2	Full QAM Capacity Utilization for DEPI	Not Possible	Possible	Possible
3	Operational Impact (wiring changes to recover from DEPI SPA failure?)	Yes	No	Minimal
4	QAM Sharing on RFGW1*	Not Possible	Possible	Possible
5	Euro-DOCSIS Impact	Yes	No	No
6	Flexbility (CMTS:EQAM Usage)	No (1:1)	Yes (1:N)	No (1:1 for Prim) Yes (1:N for backup)
7	10GE usage for DEPI on RFGW10	No	Yes	Possible
8	Hub Router (HR) Impact (e.g. 1GE ports)	No	Yes	Yes, but limited
9	Routing complexity	No	Yes	No
10	3G60 LC SPA N+1 Redundancy	No	Yes	Yes

MC3G60 with DEPI CP High Availability Prerequisites

- uBR10012 running 12.2(33)SCE1 or higher
- Global LC N+1 HCCP configured
- DEPI CP already up and running (recommended)
- MC3G60 Linecard
- uBR-RFSW
- RFGW-10 running >/= 12.2(50)SQ

MC3G60 with DEPI CP High Availability Overview

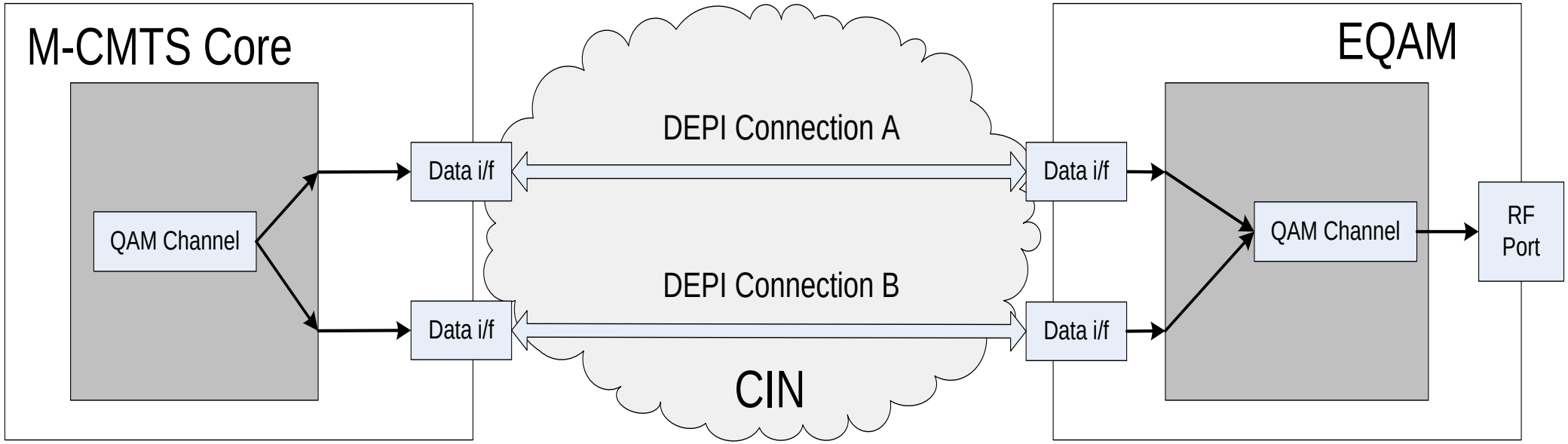
- Manual DEPI has only data path that carries DOCSIS frame
- Control Plane DEPI uses L2TPv3 signaling for setting up, maintaining, and tearing down sessions
- MC3G60 supports Manual DEPI HA
- Control Plane DEPI HA was available Q1CY11 (SCE1)
- MC3G60 supports N+1 LCHA with Manual DEPI and HCCP, or
- N+1 LCHA with Control Plane DEPI Path Redundancy (DPR) and HCCP
- PREHA, no Stateful Switchover (SSO) for control plane DEPI, but has non-stop forwarding
- GigE port redundancy, transparent to DEPI
- L3 ***indirect*** CIN not currently supported

MC3G60 Control Plane DEPI LCHA

- DEPI Path Redundancy (DPR)
  - Uses secondary tunnel/sessions to protect the corresponding primary tunnel/sessions
  - Part of the DOCSIS Downstream External PHY Interface Specification
- DPR supported by MC3G60 and RFGW-10
- If EQAM does not support DEPI DPR, manual DEPI is recommended for use with N+1
  - DPR is required to support control plane DEPI N+1 redundancy
- LCSO is triggered if network failure leads to DEPI session hello timeout
  - Replaces HCCP KA timeout failure detection
- Physical link failure, LC failure, and CLI triggered LCSO are also supported

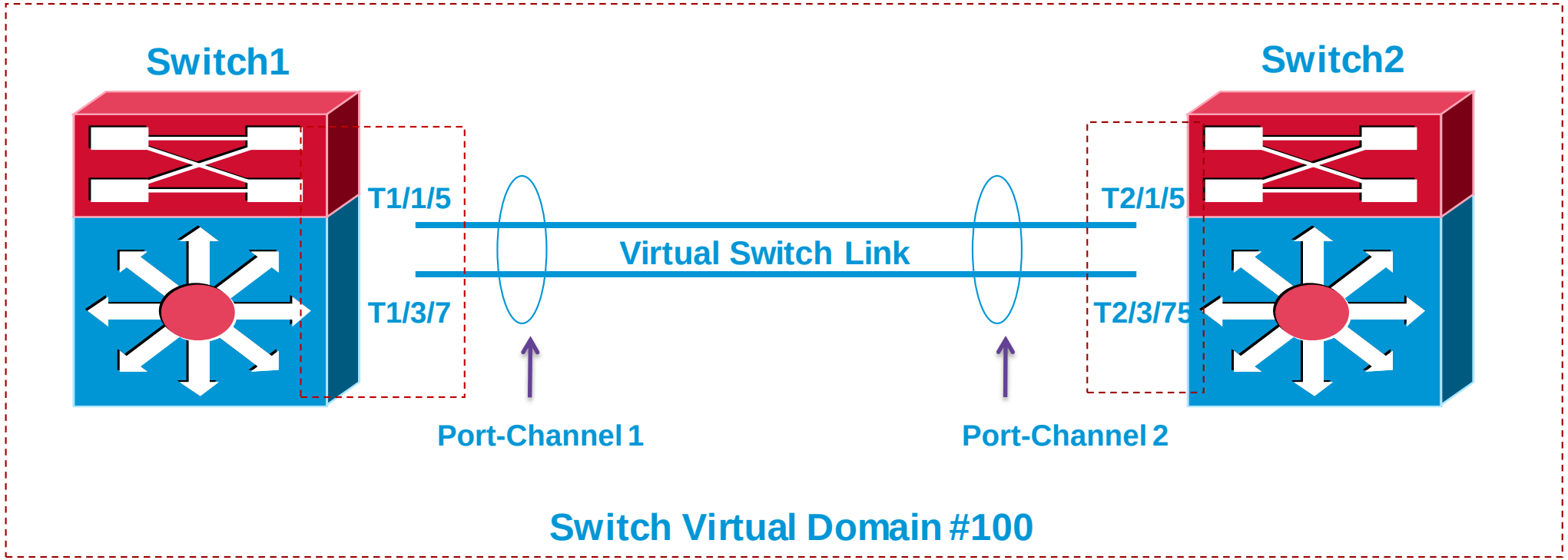
Control Plane DEPI Path Redundancy

CMTS/EQAM Block Diagram

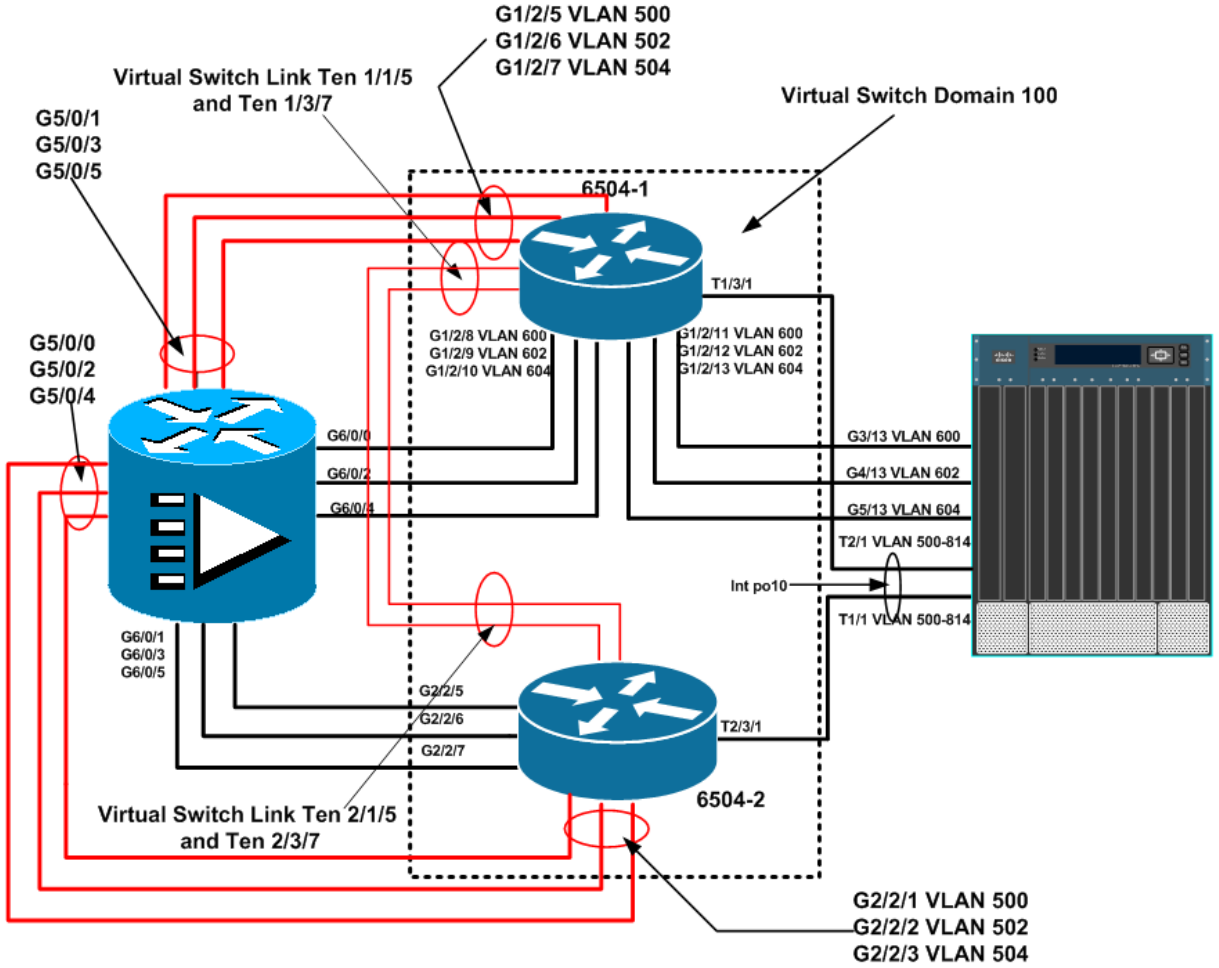


L2 CIN interconnect between CMTS and EQAM

VSS component



L2CIN evolution to scale HA and 10G



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Thank you.